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TO	Examiner Long K. Tran	September 28, 2004
NAME	U.S. PTO	DATE
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NUMBER OF PAGES INCLUDING COVER:	5	FAX #
		CONFIRM FAX: <input type="checkbox"/> YES <input checked="" type="checkbox"/> NO
FROM	Remus Fetea	245102US2SX DIV
NAME	(703) 413-2383	OUR REFERENCE
DIRECT PHONE #		10/706,970
		YOUR REFERENCE

MESSAGE

Dear Examiner Tran:

Per our earlier telephone conversation of September 28, 2004,
 enclosed please find an English translation of the Japanese Office Action dated March 30, 2004.

With best regards,

Remus F. Fetea

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(Translation)

Mailed: March 30, 2004

NOTIFICATION OF REASONS FOR REJECTION

Patent Application No.: Japanese Patent Application No. 2002-176029

Examiner's Notice Date: March 25, 2004

Examiner: M. Awano

This application is rejected on the grounds stated below. Any opinion about the rejection must be filed within THREE MONTHS of the mailing date hereof.

REASONS

1. The inventions recited in the following claims are unpatentable under Section 29 (1) (iii) of the Patent Law as being described in the following publication distributed in Japan or a foreign country prior to this application.
2. The invention recited in the following claims are unpatentable under Section 29 (2) of the Patent Law, as being such that the invention could easily have been made by a person with ordinary skill in the art to which the invention pertains, on the basis of the invention described in the following publications distributed in Japan or a foreign country prior to this application or the invention made available to the public through electric telecommunication lines in Japan or a foreign country prior to this application.
3. The inventions recited in the following claims are unpatentable under section 29^{bis} of the Patent Law on the grounds that the invention is considered the same as the invention described in the specification and the drawings originally attached to the request of the following application, which was filed before, and disclosed after, the filing date of this application and that the inventor of the present application is not considered to be the inventor of the cited application, and at the time of the filing of this application, the applicant is not considered to be the applicant of the cited application.

REMARKS

[Claims 1, 2, 6-12]

- Reasons 1 and 2
- References 1 and 2

Notification of Reasons for Rejection**Page 2/4****(Note)**

Regarding Reference 1, see FIGS. 28 and 29 and the descriptions thereof.

Regarding Reference 2, see FIG. 231 and the descriptions thereof.

· Reason 3**· References 3 and 4****(Note)**

Regarding Reference 3, see FIGS. 1-5 and the descriptions thereof.

Regarding Reference 4, see FIG. 29 and the descriptions thereof.

[Claims 4, 13 and 14]**· Reason 2****· References 1, 2, 5 and 6****(Note)**

As described in References 5 and 6, it is well known that a contact plug arranged on a gate electrode is constructed to partially overlap the gate electrode, that the cross section of the contact plug is wider than the distance to the adjacent gate electrode with the overlapping form, and that the contact plug is formed by the self-aligning method using the gate electrode. A person skilled in the art would easily apply the known means to the structure of the contact plug and the method for manufacturing the same disclosed in Reference 1 or 2, if necessary.

4. The application fails to satisfy the requirements under Section 36 (6) (i) of the Patent Law, on the grounds that the claims are defective in the following respect.

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REMARKS

In the detailed description of the invention, there is a description "the present invention has been made to solve the above problem, and its object is to provide a semiconductor device and a method for manufacturing the same, which can reduce the area occupied by a pair of capacitors on a chip by forming the pair of capacitors by one photolithography step" (see [0014]). It is considered that the means for solving the problem is "forming a pair of capacitors by one photolithography step". However, claims 1 to 14 appear to cover forming a pair of capacitors by different photolithography steps in addition to "forming a pair of capacitors by one photolithography step". Therefore, the means for solving the problem "forming a pair of capacitors by one photolithography step" described in the detailed description of the invention is not reflected in claims 1 to 14. Thus, a patent is claimed over the scope described in the detailed description of the invention.

Therefore, the inventions recited in claims 1 to 14 do not correspond to the detailed description of the invention.

The claims not mentioned in this Official Action are not rejected. If a new reason for rejection is noticed, a further Official Action will be issued.

References Cited:

1. Jpn. Pat. Appln. KOKAI Publication No. 2002-110932 (U.S. Patent No. 6,642,563)
2. Jpn. Pat. Appln. KOKAI Publication No. 2000-022010 (U.S. Patent No. 6,151,242)
3. Japanese Patent Application No. 2000-386269 (Jpn. Pat. Appln. KOKAI

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Publication No. 2002-190577) (Related U.S. Application No. 10/012,326)

4. Japanese Patent Application No. 2001-341392 (Jpn. Pat. Appln. KOKAI Publication No. 2002-217381) (U.S. Patent No. 6,680,499)
5. Jpn. Pat. Appln. KOKAI Publication No. 2000-349258
6. Jpn. Pat. Appln. KOKAI Publication No. 2000-183304

Docket No. 245102US2SX DIV

Inventor: Hiroyuki KANAYA et al

Preliminary Amendment Filed: November 14, 2003

IN THE SPECIFICATION

Please insert a new paragraph at page 1, after the title, to read as follows:

CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims benefit of priority under 35 USC §120 and is a divisional of
now Patent No. 6,677630
U.S. application serial no. 10/178,744, filed June 25, 2002, the entire contents of each of
which are incorporated herein by reference in their entirety.